

# Layouts For The Shuffle-exchange Graph And Lower Bound Techniques For VLSI (MIT/LCS/TR) By Frank Thomson Leighton

**By Frank Thomson Leighton**

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3. The Shuffle-Exchange Graph The shuffle-exchange graph on  $n$  vertices is defined only when  $n$  is a power of two. Each of the  $n/2k$  vertices can be identified with an

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Abstract: This paper describes a technique for producing a VLSI layout of the shuffle-exchange graph. It is based on the layout procedure which lays out a graph by

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Existence of Nash equilibria in selfish routing problems. Uploaded by Mimmo Parente. Info; Publisher: Springer Publication Date: Jan 1, 2004

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The shuffle exchange graph is one of the best structures known for parallel An Asymptotically Optimal Layout for the Shuffle-Exchange Graph DANIEL