

Layouts For The Shuffle-exchange Graph And Lower Bound Techniques For VLSI (MIT/LCS/TR) By Frank Thomson Leighton

By Frank Thomson Leighton

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found that the optimal shuffle-exchange (SE) graph layout from [9] applied to the implementation of Viterbi decoders

Shuffle-exchange and cube-connected cycles F.T. Leighton, M. Lepley and G.L. Miller, An asymptotically optimal layout for the shuffle-exchange graph, J

, TYPE="Technical Report" the lower bound on speedup is found to be $\alpha \times p$. , INSTITUTION="MIT Laboratory for Computer Science"

new lower bound techniques for vlsi: mit-lcs-tm-227: layouts for the shuffle-exchange graph based on the complex plane diagram: mit-lcs-tm-221: leighton, frank

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MIT-LCS-TR-695: Frank, Formal Specification Techniques for Promoting Software A FRAMEWORK FOR SOLVING VLSI GRAPH LAYOUT PROBLEMS: MIT-LCS-TR-305: Bhatt, S.N.

LAYOUTSFORTHE SHUFFLE-EXCHANGE GRAPH 203 Miller who have described optimal layouts for small shuffle-exchange graphs in [LM81]. Subsequentto

This paper studies linear layouts of generalized hypercubes, Complexity Issues in VLSI: Optimal Layouts for the Shuffle-Exchange Graph and Other Networks.

New Lower Bound Techniques for VLSI. Frank Thomson Leighton. New Layouts for the Shuffle-Exchange Graph Tom Leighton;

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Complexity Issues in VLSI. In particular, it describes optimal layouts for the shuffle-exchange graph, one of the best known networks for parallel computation.

MIT LCS Technical Memo TM-116, Frank Thomson Leighton, we present several new layouts for the shuffle-exchange graph,

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Frank Thomson Leighton; Massachusetts Institute of Technology, A new divide-and-conquer framework for VLSI graph layout is introduced.

The shuffle exchange graph is one of the best structures known for parallel An Asymptotically Optimal Layout for the Shuffle-Exchange Graph DANIEL

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